

FIG. 1

The diagram shows a differential pair circuit 44. It consists of two input transistors, Q1 and Q2, whose gates are connected to an input node 48. The sources of Q1 and Q2 are connected to a common source node 50, which is connected to ground (VSS). The drains of Q1 and Q2 are connected to a common drain node 52. The gates of Q3 and Q4 are connected to VDD. The sources of Q3 and Q4 are connected to a common source node 54, which is connected to VDD. The drains of Q3 and Q4 are connected to a common drain node 56. The gates of Q5 and Q6 are connected to VDD. The sources of Q5 and Q6 are connected to a common source node 58, which is connected to VDD. The drains of Q5 and Q6 are connected to a common drain node 60. The circuit is powered by VDD and VSS. A dashed box 46 encloses the input and current mirror sections, and a dashed box 52 encloses the output and current mirror sections.

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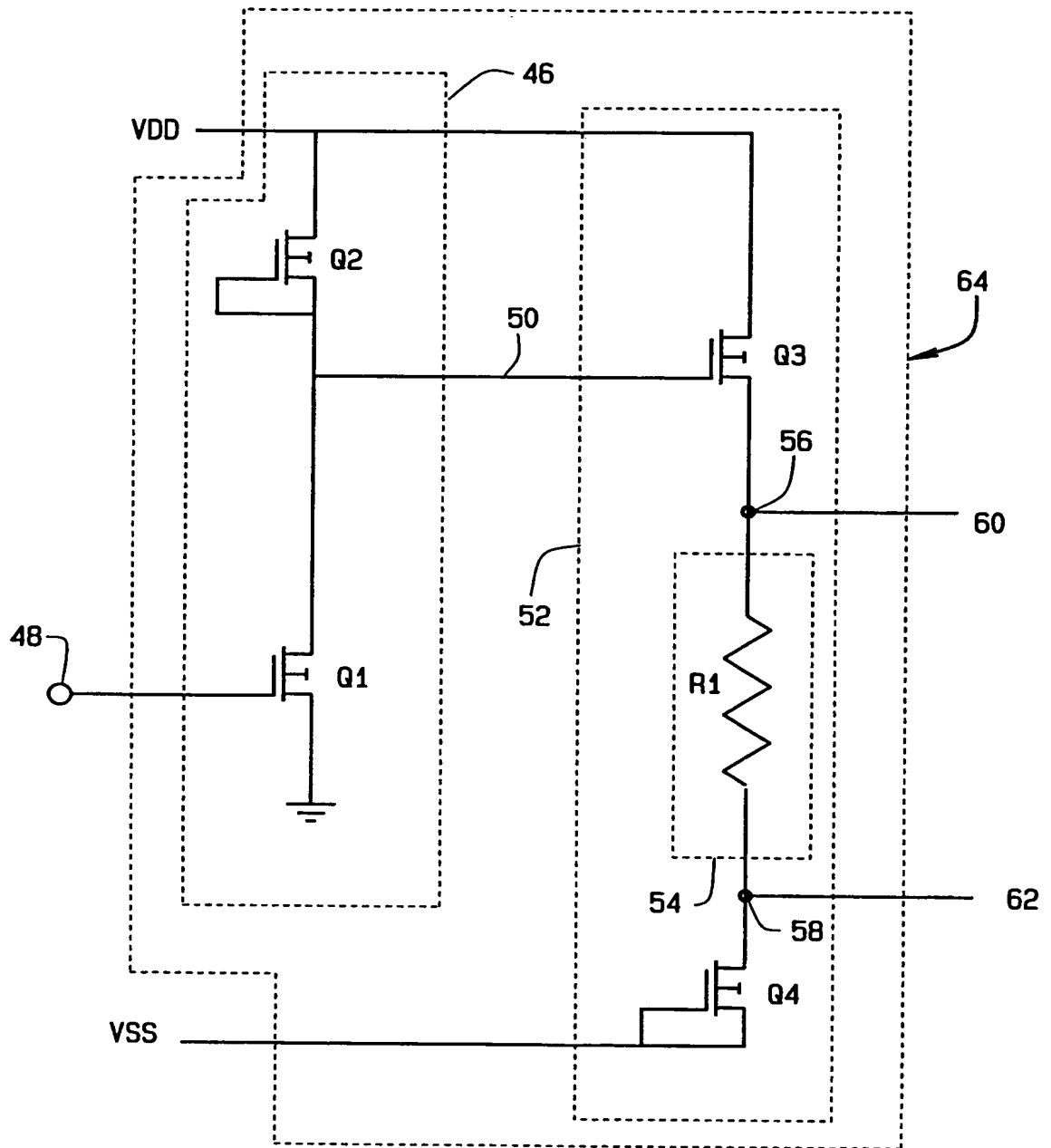


FIG. 3

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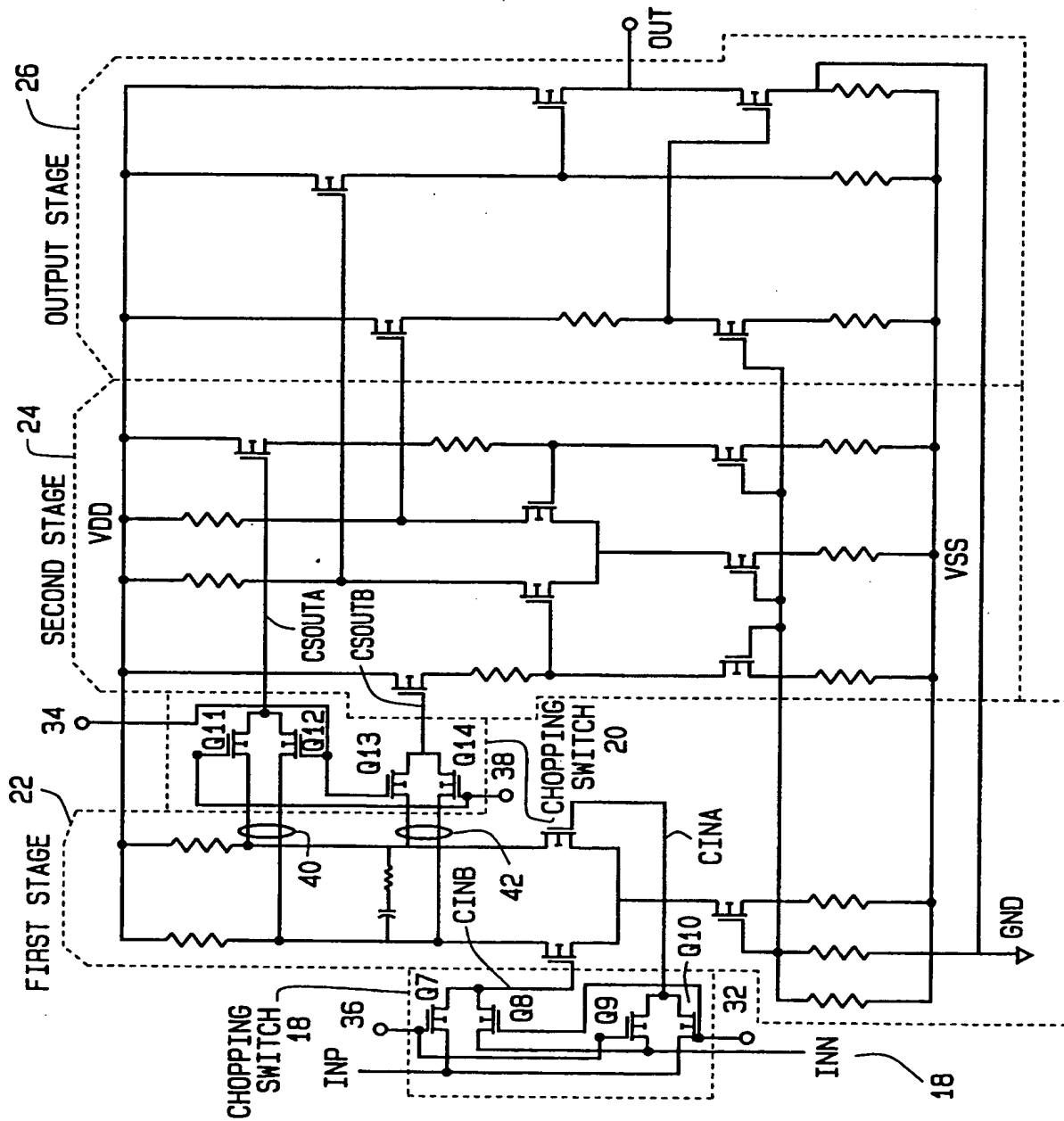


FIG. 4